

Claims

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

1. A layered structure for forming p-channel field effect transistors comprising:
  - a single crystalline substrate,
  - a first layer of relaxed  $Si_{1-x}Ge_x$  formed epitaxially on said substrate where Ge fraction  $x$  is in the range from 0.5 to 0.8,
  - a second layer of doped  $Si_{1-x}Ge_x$  formed epitaxially on said first layer,
  - a third layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said second layer,
  - a fourth layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said third layer,
  - a fifth layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said fourth layer,
  - a sixth layer of Ge formed epitaxially on said fifth layer whereby said sixth layer is under compressive strain and has a thickness less than its critical thickness with respect to the upper surface of said first layer, and
  - a seventh layer of  $Si_{1-x}Ge_x$  formed epitaxially on said sixth layer.
2. The layered structure of claim 1 further including first and second over-shoot layers,  $Si_{1-m}Ge_m$  and  $Si_{1-n}Ge_n$ , within a strain relief structure of said first layer of relaxed  $Si_{1-x}Ge_x$  for the case when  $x$  is greater than 0.5.

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3. The layered structure of claim 2 wherein said first over-shoot layer,  $\text{Si}_{1-m}\text{Ge}_m$ , within said strain relief structure of said first layer has a Ge fraction  $m$ , where  $m$  is the range from about 0.05 to less than about 0.5.

4. The layered structure of claim 2 wherein said second over-shoot layer,  $\text{Si}_{1-n}\text{Ge}_n$ , within the strain relief structure of said first layer has a Ge fraction  $n$ , where  $n = x + z$  and  $z$  is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

5. The layered structure of claim 1 wherein the active device region is a buried channel made up of an epitaxial Ge channel of said sixth layer having a higher compressive strain to provide a deeper quantum well or a higher barrier for better hole confinement with no alloy scattering as compared to a single SiGe layer channel device alone.

6. The layered structure of claim 1 wherein said sixth layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

7. The layered structure of claim 1 wherein a spacer region comprises a three layer structure of said third layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ , said fourth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ , and said fifth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ .

8. The layered structure of claim 7 wherein the Ge content of said third layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $\alpha$ , where  $\alpha = x - 0.20$  and wherein said third

layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

9. The layered structure of claim 7 wherein the Ge content of said fourth layer of  $Si_{1-x}Ge_x$  is in the range from 0.5 to 0.8 with a preferred content of  $b$ , where  $b = x - 0.25$  and wherein said fourth layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

10. The layered structure of claim 7 wherein the Ge content of said fifth layer of  $Si_{1-x}Ge_x$  is in the range from 0.5 to 0.8 with a preferred content of  $c$ , where  $c = x - 0.10$  and wherein said fifth layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

11. The layered structure of claim 1 wherein said second layer is a p-doped  $Si_{1-x}Ge_x$  layer formed below a channel region of said sixth layer and separated therefrom by said third layer of  $Si_{1-x}Ge_x$ , said fourth layer of  $Si_{1-x}Ge_x$  and said fifth layer of  $Si_{1-x}Ge_x$ , said second layer is to having a thickness in the range from 1 to 20 nm with a preferred thickness from 4 to 5 nm and said second layer having an electrically active donor dose in the range from 1 to  $4 \times 10^{12} \text{ cm}^{-2}$ .

12. The layered structure of claim 1 wherein the Ge content  $x$  may be graded within said seventh layer starting with a higher Ge content nearer said sixth layer and grading down in Ge content towards the upper surface of said seventh layer with a preferred value  $x$  of 0.30.

13. A layered structure for forming p-channel field effect transistors comprising:

a single crystalline substrate,

a first layer of relaxed  $Si_{1-x}Ge_x$  formed epitaxially on said substrate where Ge fraction  $x$  is in the range from 0.5 to 0.8,

a second layer of doped  $Si_{1-x}Ge_x$  formed epitaxially on said first layer,

a third layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said second layer,

a fourth layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said third layer,

a fifth layer of Ge formed epitaxially on said fourth layer whereby said fifth layer is under compressive strain and has a thickness less than its critical thickness with respect to said first layer, and

a sixth layer of  $Si_{1-x}Ge_x$  formed epitaxially on said fifth layer.

**14.** The layered structure of claim 13 further including two over-shoot layers,  $Si_{1-m}Ge_m$  and  $Si_{1-n}Ge_n$ , within a strain relief structure of said first layer of relaxed  $Si_{1-x}Ge_x$  for the case when  $x$  is greater than 0.5 or having a preferred value of 0.65.

**15.** The layered structure of claim 13 wherein said first over-shoot layer,  $Si_{1-m}Ge_m$ , within said strain relief structure of said first layer has a Ge fraction  $m$ , where  $m$  is the range from 0.05 to less than 0.5.

**16.** The layered structure of claim 13 wherein said second over-shoot layer,  $Si_{1-n}Ge_n$ , within the strain relief structure of said first layer has a Ge fraction  $n$ , where  $n = x + z$  and  $z$  is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

17. The layered structure of claim 13 wherein the active device region is a buried channel made up of an epitaxial Ge channel of said fifth layer having a higher compressive strain to provide a deeper quantum well or a higher barrier for better hole confinement with no alloy scattering as compared to a single SiGe layer channel device alone.

18. The layered structure of claim 13 wherein said fifth layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

19. The layered structure of claim 13 wherein a spacer region comprises a two layer structure of said third layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  and said fourth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ .

20. The layered structure of claim 13 wherein the Ge content of said third layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $a$ , where  $a = x - 0.20$  and wherein said third layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

21. The layered structure of claim 13 wherein the Ge content of said fourth layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $b$ , where  $b = x - 0.25$  and wherein said fourth layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

22. The layered structure of claim 19 wherein said spacer region comprising a two layer structure may be substituted with a single layer structure comprised of a relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer with an

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adjustable thickness to allow the spacer thickness to be varied accordingly whereby the supply dose may be optimized for device applications as a function of temperature in the range from 0.4 to 425 K.

**23.** The layered structure of claim 13 wherein said second layer is a p-doped  $\text{Si}_{1-x}\text{Ge}_x$  layer formed below a channel region of said fifth layer and separated therefrom by said third layer of  $\text{Si}_{1-x}\text{Ge}_x$ , and said fourth layer of  $\text{Si}_{1-x}\text{Ge}_x$ , said second layer having a thickness in the range from 1 to 20 nm with a preferred thickness from 4 to 5 nm and said second layer having an electrically active donor dose in the range from 1 to  $4 \times 10^{12} \text{ cm}^{-2}$ .

**24.** The layered structure of claim 22 wherein the supply layer of said second layer is formed and separated below the channel region of said fifth layer by said relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer.

**25.** The layered structure of claim 13 wherein the Ge content  $x$  may be graded within said sixth layer starting with a higher Ge content nearer said fifth layer and grading down in Ge content towards the upper surface of said sixth layer with a preferred value of 0.30.

**26.** A layered structure for forming p-channel field effect transistors comprising:

- a single crystalline substrate,
- a first layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  formed epitaxially on said substrate where Ge fraction  $x$  is in the range from 0.5 to 0.8,
- a second layer of Ge formed epitaxially on said first layer whereby said second layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,

a third layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said second layer,  
a fourth layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said third layer,  
a fifth layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said fourth layer, and  
a sixth layer of p-doped  $Si_{1-x}Ge_x$  formed epitaxially on said fifth layer.

27. The layered structure of claim 26 further including first and second over-shoot layers,  $Si_{1-m}Ge_m$  and  $Si_{1-n}Ge_n$ , within the strain relief structure of said first layer of relaxed  $Si_{1-x}Ge_x$  for the case when  $x$  is greater than 0.5 or having a preferred value of 0.65.

28. The layered structure of claim 26 wherein the first over-shoot layer,  $Si_{1-m}Ge_m$ , within a strain relief structure of said first layer has a Ge fraction  $m$ , where  $m$  is the range from 0.05 to less than 0.5.

29. The layered structure of claim 26 wherein said second over-shoot layer,  $Si_{1-n}Ge_n$ , within the strain relief structure of said first layer has a Ge fraction  $n$ , where  $n = x + z$  and  $z$  is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

30. The layered structure of claim 26 wherein the active device region is a buried channel made up of an epitaxial Ge channel of said second layer having a higher compressive strain to provide a deeper quantum well or a higher barrier for better hole confinement with no alloy scattering as compared to a single SiGe layer channel device alone.

31. The layered structure of claim 26 wherein said second layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

32. The layered structure of claim 26 wherein a spacer region comprises a three layer structure of said third layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ , said fourth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ , and said fifth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ .

33. The layered structure of claim 26 wherein the Ge content of said third layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $c$ , where  $c = x - 0.10$  and wherein said third layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

34. The layered structure of claim 26 wherein the Ge content of said fourth layer of  $\text{Si}_{1-x}\text{Ge}_x$  is the range from 0.5 to 0.8 with a preferred content of  $b$ , where  $b = x - 0.25$  and wherein said fourth layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

35. The layered structure of claim 26 wherein the Ge content of said fifth layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $a$ , where  $a = x - 0.20$  and wherein said fifth layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

36. The layered structure of claim 26 wherein said sixth layer is a p-doped  $\text{Si}_{1-x}\text{Ge}_x$  layer formed above a channel region of said second layer and separated therefrom by said third layer of  $\text{Si}_{1-x}\text{Ge}_x$ ,

said fourth layer of  $\text{Si}_{1-x}\text{Ge}_x$  and said fifth layer of  $\text{Si}_{1-x}\text{Ge}_x$ , said sixth layer having a thickness in the range from 1 to 20 nm with a preferred thickness from 4 to 5 nm and said sixth layer having an electrically active donor dose in the range from 1 to  $4 \times 10^{12} \text{ cm}^{-2}$ .

**37.** A layered structure for forming p-channel field effect transistors comprising:

a single crystalline substrate,

a first layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  formed epitaxially on said substrate where Ge fraction  $x$  is  
the range from 0.5 to 0.8,

a second layer of Ge formed epitaxially on said first layer whereby said second layer is  
under compressive strain and having a thickness less than its critical thickness  
with respect to said first layer,

a third layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  formed epitaxially on said second layer,

a fourth layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  formed epitaxially on said third layer, and

a fifth layer of p-doped  $\text{Si}_{1-x}\text{Ge}_x$  formed epitaxially on said fourth layer.

**38.** The layered structure of claim 37 further including first and second over-shoot layers,  $\text{Si}_{1-m}\text{Ge}_m$  and  $\text{Si}_{1-n}\text{Ge}_n$ , within the strain relief structure of said first layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  for the case when  $x$  is greater than 0.5.

**39.** The layered structure of claim 37 wherein the first over-shoot layer,  $\text{Si}_{1-m}\text{Ge}_m$ , within the strain relief structure of said first layer has a Ge fraction  $m$ , where  $m$  is the range from 0.05 to less than 0.5.

40. The layered structure of claim 37 wherein said second over-shoot layer,  $\text{Si}_{1-n}\text{Ge}_n$ , within the strain relief structure of said first layer has a Ge fraction  $n$ , where  $n = x + z$  and  $z$  is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

41. The layered structure of claim 37 wherein the active device region is a buried channel made up of an epitaxial Ge channel of said second layer having a higher compressive strain to provide a deeper quantum well or a higher barrier for better hole confinement with no alloy scattering as compared to a single SiGe layer channel device alone.

42. The layered structure of claim 37 wherein said second layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

43. The layered structure of claim 37 wherein a spacer region comprises a two layer structure of said third layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  and said fourth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ .

44. The layered structure of claim 37 wherein the Ge content of said third layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $c$ , where  $c = x - 0.10$  and wherein said third layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

45. The layered structure of claim 37 wherein the Ge content of said fourth layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $b$ , where  $b = x - 0.25$  and wherein said fourth

layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

46. The layered structure of claim 37 wherein said fifth layer is a p-doped  $Si_{1-x}Ge_x$  layer formed above a channel region of said second layer and separated therefrom by said third layer of  $Si_{1-x}Ge_x$  and said fourth layer of  $Si_{1-x}Ge_x$ , said fifth layer having a thickness in the range from 1 to 20 nm with a preferred thickness from 4 to 5 nm and said sixth layer having an electrically active donor dose in the range from 1 to  $4 \times 10^{12} \text{ cm}^{-2}$ .

47. The layered structure of claim 43 wherein said spacer region comprising a two layer structure may be substituted with a single layer structure comprised of a relaxed  $Si_{1-x}Ge_x$  layer with an adjustable thickness to allow the spacer thickness to be varied accordingly whereby the supply dose may be optimized for device applications as a function of temperature in the range from 0.4 to 425 K.

48. The layered structure of claim 47 wherein the supply layer of said fifth layer is formed and separated above the channel region of said second layer by said relaxed  $Si_{1-x}Ge_x$  layer.

49. The layered structure of claim 43 wherein said fourth layer of  $Si_{1-x}Ge_x$  may be substituted with a thin strained commensurate Si layer whereby a thin spacer thickness may be provided for room temperature MODFET device operation.

50. The layered structure of claim 49 wherein said fourth layer of Si is under tensile strain and is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

51. The layered structure of claim 49 wherein the supply layer of said fifth layer is formed and separated above the channel region of said second layer by said third layer of relaxed  $Si_{1-x}Ge_x$  and said fourth layer of tensilely strained Si.

52. A layered structure for forming p-channel field effect transistors comprising:

- a single crystalline substrate,
- a first layer of relaxed  $Si_{1-x}Ge_x$  formed epitaxially on said substrate where Ge fraction  $x$  is in the range from 0.5 to 0.8,
- a second layer of doped  $Si_{1-x}Ge_x$  formed epitaxially on said first layer,
- a third layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said second layer,
- a fourth layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said third layer,
- a fifth layer of Ge formed epitaxially on said fourth layer whereby said fifth layer is under compressive strain and has a thickness less than its critical thickness with respect to said first layer, and
- a sixth layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said fifth layer,
- a seventh layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said sixth layer, and
- an eighth layer of doped  $Si_{1-x}Ge_x$  formed epitaxially on said seventh layer.

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53. The layered structure of claim 52 further including first and second over-shoot layers,  $Si_{1-m}Ge_m$  and  $Si_{1-n}Ge_n$ , within a strain relief structure of said first layer of relaxed  $Si_{1-x}Ge_x$  for the case when  $x$  is greater than 0.5.

54. The layered structure of claim 52 wherein said first over-shoot layer,  $Si_{1-m}Ge_m$ , within said strain relief structure of said first layer has a Ge fraction  $m$ , where  $m$  is the range from 0.05 to less than 0.5.

55. The layered structure of claim 52 wherein said second over-shoot layer,  $Si_{1-n}Ge_n$ , within the strain relief structure of said first layer has a Ge fraction  $n$ , where  $n = x + z$  and  $z$  is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

56. The layered structure of claim 52 wherein the active device region is a buried channel made up of an epitaxial Ge channel of said fifth layer having a higher compressive strain to provide a deeper quantum well or a higher barrier for better hole confinement with no alloy scattering as compared to a single SiGe layer channel device alone.

57. The layered structure of claim 52 wherein said fifth layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

58. The layered structure of claim 52 further including first and second spacer regions whereby said first spacer region is below the Ge channel region comprising a two layer structure of said

third layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  and said fourth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ , and said second spacer region is above the active Ge channel of said fifth layer comprising a similar two layer structure of said sixth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  and said seventh layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ .

59. The layered structure of claim 58 wherein the Ge content of said third layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $a$ , where  $a = x - 0.20$  and wherein said third layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

60. The layered structure of claim 58 wherein the Ge content of said fourth layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $b$ , where  $b = x - 0.25$  and wherein said fourth layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

61. The layered structure of claim 58 wherein the Ge content of said sixth layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $c$ , where  $c = x - 0.10$  and wherein said sixth layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

62. The layered structure of claim 58 wherein the Ge content of said seventh layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $b$ , where  $b = x - 0.25$  and wherein said seventh layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

**63.** The layered structure of claim 58 wherein said spacer region comprising a two layer structure may be substituted with a single layer structure comprised of a relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer with an adjustable thickness to allow the spacer thickness to be varied accordingly whereby the supply dose may be optimized for device applications as a function of temperature in the range from 0.4 to 425 K.

**64.** The layered structure of claim 52 further including first and second supply layers whereby said first supply layer is below the Ge channel region separated by a bottom spacer region comprising a two layer structure of said third layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  and said fourth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ , and said second supply is above the active Ge channel of said fifth layer further separated by a top spacer region comprising a similar two layer structure of said sixth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  and said seventh layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ .

**65.** The layered structure of claim 52 wherein said second layer is a p-doped  $\text{Si}_{1-x}\text{Ge}_x$  layer formed below a channel region of said fifth layer and separated therefrom by said third layer of  $\text{Si}_{1-x}\text{Ge}_x$ , and said fourth layer of  $\text{Si}_{1-x}\text{Ge}_x$ , said second layer having a thickness in the range from 1 to 20 nm with a preferred thickness from 4 to 5 nm and having an electrically active donor dose in the range from 1 to  $4 \times 10^{12} \text{ cm}^{-2}$ .

**66.** The layered structure of claim 52 wherein said eight layer is a p-doped  $\text{Si}_{1-x}\text{Ge}_x$  layer formed above a channel region of said fifth layer and separated therefrom by said sixth layer of  $\text{Si}_{1-x}\text{Ge}_x$ , and said seventh layer of  $\text{Si}_{1-x}\text{Ge}_x$ , said eight layer is to having a thickness in the range from 1 to 20 nm with a preferred thickness from 4 to 5 nm and having an electrically active donor dose in the range from 1 to  $4 \times 10^{12} \text{ cm}^{-2}$ .

67. The layered structure of claim 52 wherein the supply layer of said second layer is formed and separated below the channel region of said fifth layer by a relaxed  $Si_{1-x}Ge_x$  layer.

68. The layered structure of claim 52 wherein the supply layer of said eight layer is formed and separated above the channel region of said fifth layer by a relaxed  $Si_{1-x}Ge_x$  layer.

69. A layered structure for forming p-channel field effect transistors comprising:

a single crystalline substrate,

a first layer of relaxed  $Si_{1-x}Ge_x$  formed epitaxially on said substrate where Ge fraction x is in the range from 0.5 to 0.8,

a second layer of doped  $Si_{1-x}Ge_x$  formed epitaxially on said first layer,

a third layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said second layer,

a fourth layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said third layer,

a fifth layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said fourth layer,

a sixth layer of Ge formed epitaxially on said fifth layer whereby said sixth layer is under compressive strain and has a thickness less than its critical thickness with respect to said first layer, and

a seventh layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said sixth layer,

a eighth layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said seventh layer, and

a ninth layer of doped  $Si_{1-x}Ge_x$  formed epitaxially on said eighth layer.

70. The layered structure of claim 69 further including first and second over-shoot layers,  $Si_{1-m}Ge_m$  and  $Si_{1-n}Ge_n$ , within a strain relief structure of said first layer of relaxed  $Si_{1-x}Ge_x$  for the case when  $x$  is greater than 0.5 or having a preferred value of 0.65.

71. The layered structure of claim 69 wherein said first over-shoot layer,  $Si_{1-m}Ge_m$ , within said strain relief structure of said first layer has a Ge fraction  $m$ , where  $m$  is the range from 0.05 to less than 0.5.

72. The layered structure of claim 69 wherein said second over-shoot layer,  $Si_{1-n}Ge_n$ , within the strain relief structure of said first layer has a Ge fraction  $n$ , where  $n = x + z$  and  $z$  is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

73. The layered structure of claim 69 wherein the active device region is a buried channel made up of an epitaxial Ge channel of said sixth layer having a higher compressive strain to provide a deeper quantum well or a higher barrier for better hole confinement with no alloy scattering as compared to a single SiGe layer channel device alone.

74. The layered structure of claim 69 wherein said sixth layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

75. The layered structure of claim 69 further including first and second spacer regions whereby said first spacer region is below the Ge channel region comprising a three layer structure of said

third layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ , said fourth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  and said fifth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ , and the second spacer region is above the active Ge channel of said sixth layer comprising a dissimilar two layer structure of said seventh layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  and said eighth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ .

76. The layered structure of claim 69 wherein the Ge content of said third layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $a$ , where  $a = x - 0.20$  and wherein said third layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

77. The layered structure of claim 69 wherein the Ge content of said fourth layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $b$ , where  $b = x - 0.25$  and wherein said fourth layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

78. The layered structure of claim 69 wherein the Ge content of said fifth layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $c$ , where  $c = x - 0.10$  and wherein said fifth layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

79. The layered structure of claim 69 wherein the Ge content of said seventh layer of  $\text{Si}_{1-x}\text{Ge}_x$  is in the range from 0.5 to 0.8 with a preferred content of  $c$ , where  $c = x - 0.10$  and wherein said seventh layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

80. The layered structure of claim 69 wherein the Ge content of said eighth layer of  $\text{Si}_{1-x}\text{Ge}_x$  is the range from 0.5 to 0.8 with a preferred content of  $b$ , where  $b = x - 0.25$  and wherein said eighth layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

81. The layered structure of claim 75 wherein said bottom spacer region comprising a three layer structure may be substituted with a single layer structure comprised of a relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer with an adjustable thickness to allow the spacer thickness to be varied accordingly whereby the supply dose may be optimized for device applications as a function of temperature in the range from 0.4 to 425 K.

82. The layered structure of claim 75 wherein said top spacer region comprising a two layer structure may be substituted with a single layer structure comprised of a relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer with an adjustable thickness to allow the spacer thickness to be varied accordingly whereby the supply dose may be optimized for device applications as a function of temperature in the range from 0.4 to 425 K.

83. The layered structure of claim 75 wherein said both top and bottom spacer regions may be substituted with a single layer structure comprised of a relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer with an adjustable thickness to allow the spacer thickness to be varied accordingly whereby the supply dose may be optimized for device applications as a function of temperature in the range from 0.4 to 425 K.

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84. The layered structure of claim 69 further including first and second supply layers whereby said first supply layer is below the Ge channel region separated by a bottom spacer region comprising a three layer structure of said third layer of relaxed  $Si_{1-x}Ge_x$ , said fourth layer of relaxed  $Si_{1-x}Ge_x$  and said fifth layer of relaxed  $Si_{1-x}Ge_x$ , and said second supply is above the active Ge channel of said sixth layer further separated by a top spacer region comprising a dissimilar two layer structure of said seventh layer of relaxed  $Si_{1-x}Ge_x$  and said eighth layer of relaxed  $Si_{1-x}Ge_x$ .

85. The layered structure of claim 69 wherein said second layer is a p-doped  $\text{Si}_{1-x}\text{Ge}_x$  layer formed below a channel region of said sixth layer and separated therefrom by said third layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ , said fourth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  and said fifth layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ , said second layer having a thickness in the range from 1 to 20 nm with a preferred thickness from 4 to 5 nm and having an electrically active donor dose in the range from 1 to  $4 \times 10^{12} \text{ cm}^{-2}$ .

**86.** The layered structure of claim 69 wherein said ninth layer is a p-doped  $\text{Si}_{1-x}\text{Ge}_x$  layer formed above a channel region of said sixth layer and separated therefrom by said seventh layer of  $\text{Si}_{1-x}\text{Ge}_x$ , and said eighth layer of  $\text{Si}_{1-x}\text{Ge}_x$ , said ninth layer is to having a thickness in the range from 1 to 20 nm with a preferred thickness from 4 to 5 nm and having an electrically active donor dose in the range from 1 to  $4 \times 10^{12} \text{ cm}^{-2}$ .

87. The layered structure of claim 69 wherein the supply layer of said second layer is formed and separated below the channel region of said fifth layer by a relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer.

**88.** The layered structure of claim 69 wherein the supply layer of said eight layer is formed and separated above the channel region of said fifth layer by a relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer.

89. A layered structure for forming a Ge channel field effect transistors comprising:

- a single crystalline substrate,
- a first layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  formed epitaxially on said substrate where Ge fraction  $x$  is in the range from 0.5 to 0.8,
- a second layer of Ge formed epitaxially on said first layer whereby said second layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,
- a third layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  formed epitaxially on said second layer, and
- a fourth layer of gate dielectric formed on said third layer.

90. The layered structure of claim 89 further including first and second over-shoot layers,  $\text{Si}_{1-m}\text{Ge}_m$  and  $\text{Si}_{1-n}\text{Ge}_n$ , within a strain relief structure of said first layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  for the case when  $x$  is greater than 0.5.

91. The layered structure of claim 89 wherein said first over-shoot layer,  $\text{Si}_{1-m}\text{Ge}_m$ , within said strain relief structure of said first layer has a Ge fraction  $m$ , where  $m$  is the range from 0.05 to less than 0.5.

92. The layered structure of claim 89 wherein said second over-shoot layer,  $\text{Si}_{1-n}\text{Ge}_n$ , within the strain relief structure of said first layer has a Ge fraction  $n$ , where  $n = x + z$  and  $z$  is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

93. The layered structure of claim 89 wherein the active device region is a buried channel made up of an epitaxial Ge channel of said second layer having a higher compressive strain to provide a deeper quantum well or a higher barrier for better hole confinement with no alloy scattering as compared to a single SiGe layer channel device alone.

94. The layered structure of claim 89 wherein the Ge content of said third layer of  $Si_{1-x}Ge_x$  is in the range from 0.5 to 0.8 with a preferred content of 0.30 and wherein said third layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer with a thickness equal to or less than 1 nm.

95. The layered structure of claim 89 wherein the Ge content x may be graded within said third layer starting with a higher Ge content nearer said second layer and grading down in Ge content towards the upper surface of said third layer to a value of about 0.30.

96. The layered structure of claim 89 wherein the gate dielectric of said fourth layer is a dielectric material selected from the group consisting of silicon dioxide, silicon oxynitride, silicon nitride, tantalum oxide, barium strontium titanate, aluminum oxide and combinations thereof.

97. The layered structure of claim 89 wherein said third layer of  $Si_{1-x}Ge_x$  may be substituted with a thin strained commensurate Si layer suitable for high temperature oxidation in formation of a high quality silicon dioxide layer in said fourth layer of gate dielectric.

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98. The layered structure of claim 97 wherein said third layer of Si is under tensile strain and is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

99. A layered structure for forming a Ge channel field effect transistor comprising:

- a single crystalline substrate,
- a first layer of relaxed  $Si_{1-x}Ge_x$  formed epitaxially on said substrate where Ge fraction  $x$  is the range from 0.5 to 0.8,
- a second layer of Ge formed epitaxially on said first layer whereby said second layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,
- a third layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said second layer,
- a fourth layer of undoped Si formed epitaxially on said third layer, and
- a fifth layer of gate dielectric formed on said fourth layer.

100. The layered structure of claim 99 further including first and second over-shoot layers,  $Si_{1-m}Ge_m$  and  $Si_{1-n}Ge_n$ , within a strain relief structure of said first layer of relaxed  $Si_{1-x}Ge_x$  for the case when  $x$  is greater than 0.5.

101. The layered structure of claim 99 wherein said first over-shoot layer,  $Si_{1-m}Ge_m$ , within said strain relief structure of said first layer has a Ge fraction  $m$ , where  $m$  is the range from 0.05 to less than 0.5.

102. The layered structure of claim 99 wherein said second over-shoot layer,  $Si_{1-n}Ge_n$ , within the strain relief structure of said first layer has a Ge fraction  $n$ , where  $n = x + z$  and  $z$  is in the range

from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

**103.** The layered structure of claim 99 wherein the active device region is a buried channel made up of an epitaxial Ge channel of said second layer having a higher compressive strain to provide a deeper quantum well or a higher barrier for better hole confinement with no alloy scattering as compared to a single SiGe layer channel device alone.

**104.** The layered structure of claim 99 wherein said second layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

**105.** The layered structure of claim 99 wherein the Ge content of said third layer of  $Si_{1-x}Ge_x$  is in the range from 0.5 to 0.8 with a preferred content of 0.30 and wherein said third layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer with a thickness equal to or less than 1 nm.

**106.** The layered structure of claim 99 wherein the Ge content x may be graded within said third layer starting with a higher Ge content nearer said second layer and grading down in Ge content towards the upper surface of said third layer to a value of about 0.30.

**107.** The layered structure of claim 99 wherein the gate dielectric of said fourth layer is a dielectric material selected from the group consisting of silicon dioxide, silicon oxynitride, silicon nitride, tantalum oxide, barium strontium titanate, aluminum oxide and combinations thereof.

108. The layered structure of claim 99 wherein said third layer of  $Si_{1-x}Ge_x$  may be substituted with a thin strained commensurate Si layer suitable for high temperature oxidation in formation of a high quality silicon dioxide layer in said fourth layer of gate dielectric.

109. The layered structure of claim 99 wherein said fourth layer of Si is under tensile strain and is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

110. A layered structure for forming a field effect transistor comprising:

- a single crystalline substrate,
- a first layer of relaxed  $Si_{1-x}Ge_x$  formed epitaxially on said substrate where Ge fraction  $x$  is the range from 0.5 to 0.8,
- a second layer of Ge formed epitaxially on said first layer whereby said second layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,
- a third layer of undoped  $Si_{1-x}Ge_x$  formed epitaxially on said second layer,
- a first Schottky gate electrode formed on said third layer,
- a first source region of a first type formed and located on one side of said first gate electrode, and
- a first drain region of a first type formed and located on the other side of said first gate electrode whereby a first field-effect transistor structure is formed of a first type.

**111.** The layered structure of claim 110 further including,

electrical isolation regions created by the selective removal of at least said third layer through said second layer,

a second Schottky gate electrode formed on said third layer positioned with respect to said electrical isolation regions to be electrically isolated from said first field-effect transistor structure,

a second source region of a second type formed and located on one side of said second gate electrode, and

a second drain region of a second type formed and located on the other side of said second gate electrode whereby a second field-effect transistor structure is formed of a second type.

**112.** The layered structure of claim 1 further including,

electrical isolation regions created by the selective removal of at least said seventh layer through said second layer,

a Schottky gate electrode formed on said seventh layer,

a source electrode formed and located on one side of said gate electrode, and

a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed.

**113.** The layered structure of claim 13 further including,

electrical isolation regions created by the selective removal of at least said sixth layer through said second layer,

a Schottky gate electrode formed on said sixth layer,

a source electrode formed and located on one side of said gate electrode, and

a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed.

**114.** The layered structure of claim 26 further including,

electrical isolation regions created by the selective removal of at least said sixth layer through said second layer,

a Schottky gate electrode formed on said sixth layer,

a source electrode formed and located on one side of said gate electrode, and

a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed.

**115.** The layered structure of claim 37 further including,

electrical isolation regions created by the selective removal of at least said fifth layer through said second layer,

a Schottky gate electrode formed on said fifth layer,

a source electrode formed and located on one side of said gate electrode, and

a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed.

**116.** The layered structure of claim 52 further including,

electrical isolation regions created by the selective removal of at least said seventh layer through said second layer,

a Schottky gate electrode formed on said seventh layer,

a source electrode formed and located on one side of said gate electrode, and

a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed.

**117.** The layered structure of claim 69 further including,  
electrical isolation regions created by the selective removal of at least said eighth  
layer through said second layer,  
a Schottky gate electrode formed on said eighth layer,  
a source electrode formed and located on one side of said gate electrode, and  
a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed.

**118.** The layered structure of claim 1 further including,  
electrical isolation regions created by the selective removal of at least said seventh  
layer through said second layer,  
a gate dielectric formed on said seventh layer,  
a gate electrode formed on said gate dielectric,  
a source electrode formed and located on one side of said gate electrode, and  
a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed.

**119.** The layered structure of claim 13 further including,  
electrical isolation regions created by the selective removal of at least said sixth  
layer through said second layer,  
a gate dielectric formed on said sixth layer,

a gate electrode formed on said gate dielectric,  
a source electrode formed and located on one side of said gate electrode, and  
a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed.

**120.** The layered structure of claim 26 further including,

electrical isolation regions created by the selective removal of at least said sixth layer through said second layer,  
a gate dielectric formed on said sixth layer,  
a gate electrode formed on said gate dielectric,  
a source electrode formed and located on one side of said gate electrode, and  
a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed.

**121.** The layered structure of claim 37 further including,

electrical isolation regions created by the selective removal of at least said fifth layer through said second layer,  
a gate dielectric formed on said fifth layer,  
a gate electrode formed on said gate dielectric,  
a source electrode formed and located on one side of said gate electrode, and  
a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed.

122. The layered structure of claim 52 further including,  
electrical isolation regions created by the selective removal of at least said seventh  
layer through said second layer,  
a gate dielectric formed on said seventh layer,  
a gate electrode formed on said gate dielectric,  
a source electrode formed and located on one side of said gate electrode, and  
a drain electrode formed and located on the other side of said gate electrode whereby a  
field-effect transistor structure is formed.

123. The layered structure of claim 69 further including,  
electrical isolation regions created by the selective removal of at least said eighth  
layer through said second layer,  
a gate dielectric formed on said eighth layer,  
a gate electrode formed on said gate dielectric,  
a source electrode formed and located on one side of said gate electrode, and  
a drain electrode formed and located on the other side of said gate electrode whereby a  
field-effect transistor structure is formed.

124. The layered structure of claim 89 further including,  
electrical isolation regions created by the selective removal of at least said fourth layer  
through said second layer,  
a gate electrode formed on said gate dielectric of said fourth layer,  
a source electrode formed and located on one side of said gate electrode, and

a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed.

125. The layered structure of claim 99 further including,

electrical isolation regions created by the selective removal of at least said fifth layer through said second layer,

a gate electrode formed on said gate dielectric of said fifth layer,

a source electrode formed and located on one side of said gate electrode, and

a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed.

126. A method for forming p-channel field effect transistors comprising the steps of:

selecting a single crystalline substrate,

forming a first layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said substrate where Ge fraction  $x$  is

in the range from 0.5 to 0.8,

forming a second layer of doped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said first layer,

forming a third layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said second layer,

forming a fourth layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said third layer,

forming a fifth layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said fourth layer,

forming a sixth layer of Ge epitaxially on said fifth layer whereby said

compressive strain and has a thickness less than its critical thickness with respect to the upper surface of said first layer, and

forming a seventh layer of  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said sixth layer.

127. The method of claim 126 further including the steps of forming first and second over-shoot layers,  $Si_{1-m}Ge_m$  and  $Si_{1-n}Ge_n$ , within a strain relief structure of said first layer of relaxed  $Si_{1-x}Ge_x$  for the case when  $x$  is greater than 0.5.

128. The method of claim 127 wherein said step of forming said first over-shoot layer,  $Si_{1-m}Ge_m$ , within said strain relief structure of said first layer includes forming a Ge fraction  $m$ , where  $m$  is the range from about 0.05 to less than about 0.5.

129. The method of claim 127 wherein said step of forming said second over-shoot layer,  $Si_{1-n}Ge_n$ , within the strain relief structure of said first layer includes forming a Ge fraction  $n$ , where  $n = x + z$  and  $z$  is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

130. A method for forming p-channel field effect transistors comprising the steps of:

- selecting a single crystalline substrate,
- forming a first layer of relaxed  $Si_{1-x}Ge_x$  epitaxially on said substrate where Ge fraction  $x$  is in the range from 0.5 to 0.8,
- forming a second layer of doped  $Si_{1-x}Ge_x$  epitaxially on said first layer,
- forming a third layer of undoped  $Si_{1-x}Ge_x$  epitaxially on said second layer,
- forming a fourth layer of undoped  $Si_{1-x}Ge_x$  epitaxially on said third layer,
- forming a fifth layer of Ge epitaxially on said fourth layer whereby said fifth layer is under compressive strain and has a thickness less than its critical thickness with respect to said first layer, and
- forming a sixth layer of  $Si_{1-x}Ge_x$  epitaxially on said fifth layer.

131. A method for forming p-channel field effect transistors comprising the steps of:

- selecting a single crystalline substrate
- forming a first layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said substrate where Ge fraction  $x$  is the range from 0.5 to 0.8,
- forming a second layer of Ge epitaxially on said first layer whereby said second layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,
- forming a third layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said second layer,
- forming a fourth layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said third layer,
- forming a fifth layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said fourth layer, and
- forming a sixth layer of p-doped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said fifth layer.

132. A method for forming p-channel field effect transistors comprising the steps of:

- selecting a single crystalline substrate,
- forming a first layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said substrate where Ge fraction  $x$  is the range from 0.5 to 0.8,
- forming a second layer of Ge epitaxially on said first layer whereby said second layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,
- forming a third layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said second layer,
- forming a fourth layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said third layer, and
- forming a fifth layer of p-doped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said fourth layer.

133. A method for forming p-channel field effect transistors comprising the steps of:

- selecting a single crystalline substrate,
- forming a first layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said substrate where Ge fraction  $x$  is in the range from 0.5 to 0.8,
- forming a second layer of doped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said first layer,
- forming a third layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said second layer,
- forming a fourth layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said third layer,
- forming a fifth layer of Ge epitaxially on said fourth layer whereby said fifth layer is under compressive strain and has a thickness less than its critical thickness with respect to said first layer, and
- forming a sixth layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said fifth layer,
- forming a seventh layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said sixth layer, and
- forming an eighth layer of doped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said seventh layer.

134. A method for forming p-channel field effect transistors comprising the steps of:

- selecting a single crystalline substrate,
- forming a first layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said substrate where Ge fraction  $x$  is in the range from 0.5 to 0.8,
- forming a second layer of doped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said first layer,
- forming a third layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said second layer,
- forming a fourth layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said third layer,
- forming a fifth layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said fourth layer,
- forming a sixth layer of Ge epitaxially on said fifth layer whereby said sixth layer is under compressive strain and has a thickness less than its critical thickness with

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respect to said first layer, and

forming a seventh layer of undoped  $Si_{1-x}Ge_x$  epitaxially on said sixth layer,

forming a eighth layer of undoped  $Si_{1-x}Ge_x$  epitaxially on said seventh layer, and

forming a ninth layer of doped  $Si_{1-x}Ge_x$  epitaxially on said eighth layer.

**135.** A method for forming a Ge channel field effect transistor comprising the steps of:

selecting a single crystalline substrate,

forming a first layer of relaxed  $Si_{1-x}Ge_x$  epitaxially on said substrate where Ge fraction  $x$  is the range from 0.5 to 0.8,

forming a second layer of Ge epitaxially on said first layer whereby said second layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,

forming a third layer of undoped  $Si_{1-x}Ge_x$  epitaxially on said second layer, and

forming a fourth layer of gate dielectric on said third layer.

**136.** A method for forming a Ge channel field effect transistor comprising the steps of:

selecting a single crystalline substrate,

forming a first layer of relaxed  $Si_{1-x}Ge_x$  epitaxially on said substrate where Ge fraction  $x$  is the range from 0.5 to 0.8,

forming a second layer of Ge epitaxially on said first layer whereby said second layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,

forming a third layer of undoped  $Si_{1-x}Ge_x$  epitaxially on said second layer,

forming a fourth layer of undoped Si epitaxially on said third layer, and

forming a fifth layer of gate dielectric on said fourth layer.

137. A method for forming a field effect transistor comprising the steps of:

- selecting a single crystalline substrate,
- forming a first layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said substrate where Ge fraction x is the range from 0.5 to 0.8,
- forming a second layer of Ge epitaxially on said first layer whereby said second layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,
- forming a third layer of undoped  $\text{Si}_{1-x}\text{Ge}_x$  epitaxially on said second layer,
- forming a first Schottky gate electrode on said third layer,
- forming a first source region of a first type and located on one side of said first gate electrode, and
- forming a first drain region of a first type and located on the other side of said first gate electrode whereby a first field-effect transistor structure is formed of a first type.

138. The method of claim 137 further including the steps of,

- forming electrical isolation regions by the selective removal of at least said third layer through said second layer,
- forming a second Schottky gate electrode on said third layer positioned with respect to said electrical isolation regions to be electrically isolated from said first field-effect transistor structure,
- forming a second source region of a second type and located on one side of said second gate electrode, and

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forming a second drain region of a second type and located on the other side of said second gate electrode whereby a second field-effect transistor structure is formed of a second type.

139. The method of claim 126 further including the steps of,  
forming a first Schottky gate electrode on said seventh layer,  
forming a first source electrode and located on one side of said first gate electrode, and  
forming a first drain electrode and located on the other side of said first gate electrode  
whereby a first field-effect transistor structure is formed.

140. The method of claim 139 further including the steps of,  
forming electrical isolation regions by the selective removal of at least said seventh  
layer through said second layer,  
forming a second gate dielectric on said seventh layer,  
forming a second gate electrode on said gate dielectric,  
forming a second source electrode and located on one side of said second gate electrode,  
and  
forming a second drain electrode on the other side of said second gate electrode whereby a  
second field-effect transistor structure is formed.